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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/023,234	02/13/1998	THOMAS J. HOLMAN	042390P5658	6664

7590 03/24/2004

BLAKELY SOKOLOFF TAYLOR& ZAFMAN
12400 WILSHIRE BOULEVARD 7TH FLOOR
LOS ANGELES, CA 90025

EXAMINER	
VERBRUGGE, KEVIN	
ART UNIT	**PAPER NUMBER**
2188	29

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/023,234	HOLMAN, THOMAS J.	
	Examiner	Art Unit	
	Kevin Verbrugge	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/12/04 has been entered.

Response to Amendment

This final Office action is in response to Amendment E, paper #27, and the terminal disclaimer, paper #28, both filed 3/12/04 by fax with the RCE mentioned above. The amendment amended claims 18 and 21. Claims 18-30 are pending. All objections and rejections not repeated below are withdrawn.

Claim Objections

Claim 18 is objected to because of the following informalities: in line 3, --controller-- should be reinserted after "module" to correct a presumably inadvertent omission. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 18-21, 23, 24, 27, and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 4,045,781 to Levy et al., hereinafter simply Levy.

Regarding claim 18, Levy discloses memory modules with selectable byte addressing for a digital data processing system.

Levy shows the claimed plurality of memory devices as low stacks 44 and high stacks 45 in Fig. 1.

He shows the claimed memory module controller as memory transceiver 41 and memory control and timing circuit 42.

He shows the claimed system memory controller as memory management unit 22 and the claimed system memory bus as memory bus 40.

Levy's memory module controller (memory transceiver 41 and memory control and timing circuit 42) operates as claimed, serving as an interface between the plurality of memory devices and the system memory bus such that the plurality of memory devices and the system memory bus operate in different operating environments. Furthermore, the memory module controller separates the plurality of memory devices from the system memory controller and the system memory bus as newly claimed.

Regarding claim 19, Levy's memory control and timing circuit 42 includes the claimed clock generator since it generates a clock signal to drive the separate signals controlling the plurality of memory devices as claimed. Fig. 11 shows memory control

and timing circuit 42 in detail, including control signal generator 145 (which outputs CLK MDR BYTE 0-3 signals), read timing generator 152, and write timing generator 156.

Regarding claim 20, Levy's memory module controller includes the claimed request handling logic since it examines a memory request to determine whether the memory request is addressed to the memory devices in its module and ignores the request if it is not addressed to its memory devices as claimed.

Regarding claim 21, Levy's memory module controller comprises the claimed power management unit because it controls power supplied to the memory devices as claimed. Levy's memory transceiver 41 and memory control and timing circuit 42 control all the signals and data supplied to the memory devices and thereby control the power supplied to the memory devices since power is transmitted on signals. In other words, power in the form of data, control, and timing signals is supplied to the memory devices. The broad language of the claim requires nothing more.

Regarding claim 23, since Levy's memory module controller does not send signals to its memory devices when a memory request is not addressed to any of the devices, it can be said that the memory controller reduces the power to the memory devices (since power is transmitted on the signals, as discussed in the rejection of claim 21 above).

Regarding claim 24, since Levy's memory module controller does not send signals to its memory devices when a memory request is not addressed to any of the devices, it can be said that the memory controller decouples the memory devices from the memory bus.

Regarding claim 27, Levy shows the claimed bus as the low bus (data), high bus (data), and control and timing signals bus in Fig. 1.

Regarding claim 30, Levy's memory devices are volatile.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 22, 25, 26, 28, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,045,781 to Levy et al.

Regarding claim 22, Levy does not teach that his memory devices and the memory bus operate at different voltages. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Levy's device to have the memory devices and the memory bus operate at different voltages to save

power. It was well-known in the art at the time of the invention that operating devices at lower voltages reduces the total amount of power consumed, therefore the skilled artisan who was interested in saving the most power would have been motivated to design each component of the system to operate at the lowest possible voltage, thereby motivating him to modify Levy's device so the memory bus and the memory devices operated at different voltages.

Regarding claim 25, Levy does not teach altering the frequency of a clock signal to the memory devices when a memory request is not addressed to any of the memory devices on a particular module, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to do just that in order to save power.

Regarding claim 26, Levy does not teach disabling his clock generator when a memory request is not addressed to any of the memory devices on a particular module, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to do just that in order to save power.

Regarding claims 28 and 29, Levy does not disclose that his memory modules are SIMMs or DIMMs, perhaps because such terms were not used in the art at the time of his disclosure. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement his memory modules as SIMMs and

DIMMs since those types of memory modules were common at the time of the invention.

****

Claims 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,045,781 to Levy et al. in view of U.S. Patent 5,257,233 to Schaefer.

Regarding claims 21, 23, and 24, Levy does not explicitly teach that his memory module controller comprises a power management unit.

Schaefer discloses a low power memory module using restricted RAM activation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include Schaefer's power reduction circuitry and techniques in Levy's memory modules to reduce the amount of power consumed. Schaefer teaches that unused memory devices may be powered down or placed in a reduced power mode to reduce the amount of power consumed by the module as a whole. By powering down certain memory devices, they are effectively decoupled from the memory bus.

Regarding claim 22, neither Levy nor Schaefer teach that their memory devices and the memory bus operate at different voltages. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Levy's device to

have the memory devices and the memory bus operate at different voltages to save power. It was well-known in the art at the time of the invention that operating devices at lower voltages reduces the total amount of power consumed, therefore the skilled artisan who was interested in saving the most power would have been motivated to design each component of the system to operate at the lowest possible voltage, thereby motivating him to modify Levy's device so the memory bus and the memory devices operated at different voltages.

Regarding claim 25, Levy does not teach altering the frequency of a clock signal to the memory devices when a memory request is not addressed to any of the memory devices on a particular module, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to do just that in order to save power.

Regarding claim 26, Levy does not teach disabling his clock generator when a memory request is not addressed to any of the memory devices on a particular module, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to do just that in order to save power.

****

Claims 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,045,781 to Levy et al. in view of U.S. Patent 5,036,493 to Nielsen.

Regarding claims 21, 23, and 24, Levy does not explicitly teach that his memory module controller comprises a power management unit.

Nielsen discloses a system and method for reducing power usage by multiple memory modules.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include Nielsen's power reduction circuitry and techniques in Levy's memory modules to reduce the amount of power consumed. Nielsen teaches that unused memory devices may be powered down or placed in a reduced power mode to reduce the amount of power consumed by the module as a whole. By powering down certain memory devices, they are effectively decoupled from the memory bus.

Regarding claim 22, neither Levy nor Nielsen teach that their memory devices and the memory bus operate at different voltages. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Levy's device to have the memory devices and the memory bus operate at different voltages to save power. It was well-known in the art at the time of the invention that operating devices at lower voltages reduces the total amount of power consumed, therefore the skilled artisan who was interested in saving the most power would have been motivated to design each component of the system to operate at the lowest possible voltage, thereby

motivating him to modify Levy's device so the memory bus and the memory devices operated at different voltages.

Regarding claim 25, Levy does not teach altering the frequency of a clock signal to the memory devices when a memory request is not addressed to any of the memory devices on a particular module, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to do just that in order to save power.

Regarding claim 26, Levy does not teach disabling his clock generator when a memory request is not addressed to any of the memory devices on a particular module, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to do just that in order to save power.

Response to Arguments

On page 6 of the amendment, first paragraph, Applicant argues that "Claim 18 as [sic] presently amended to more clearly claim that the memory module controller serves as a direct interface to the system memory controller." However, the claim actually reads "the memory module controller . . . serves as a direct interface between the plurality of the memory devices and the system memory bus."

While it may be true that Levy's memory module controller (memory transceiver 41 and memory control and timing unit 42) does not serve as a direct interface to his system memory controller (memory management unit 22), it is certainly true that his

memory module controller serves as a direct interface between the plurality of the memory devices (low stack units 44 and high stack units 45) and the system memory bus (memory bus 40), as claimed, therefore the rejection is maintained and made final.

If Applicant wishes to claim the limitation presented in the arguments (that the memory module controller serves as a direct interface to the system memory controller), then the claim must be amended accordingly. However, it should be noted that the claim as currently written is supported by the specification, such as Fig. 3, which shows a memory module controller 316 serving as a direct interface between memory devices 317-320 and the system memory bus 323. Therefore, any claim amendment which specified that the memory module controller served as a direct interface to the system memory controller would be understood to mean that the memory module controller served as a direct interface to a system memory bus which is connected to a system memory controller.

In any case, it is not at all clear to the Examiner that it would be inappropriate to characterize Levy's system memory controller as including memory management unit 22 and associative memory 24, since the associative memory 24 apparently performs some memory control functions (see column 7, lines 9-10, for example, where Levy teaches that "associative memory 24 initiates a memory cycle").

In other words, the claims as amended are still anticipated by Levy since his memory module controller serves as a direct interface to the system memory bus. Furthermore, should Applicant amend the claims to indicate that the memory module controller serves as a direct interface to the system memory controller, it is possible that

Levy's associative memory could be considered as part of his system memory controller, and therefore Levy's disclosure would still anticipate the claimed invention.

At page 6, second paragraph, second sentence, Applicant asserts "that Levy does not teach interfacing a system memory controller to a memory management unit." The Examiner had never asserted such, rather the Examiner is characterizing Levy's memory management unit as his system memory controller. Perhaps Applicant meant that Levy does not teach interfacing a system memory controller to a memory module controller, but this is contradicted by the rest of Applicant's sentence where he asserts that Levy "teaches using an intermediate associative memory to interface a memory management unit to the memory control and timing/memory transceiver combination," which means that Levy's memory management unit (system memory controller) does interface to his memory control and timing/memory transceiver combination (memory module controller), albeit indirectly, using an associative memory.

What is apparently being argued by Applicant is that Levy's system memory controller does not interface directly to his memory module controller but rather indirectly interfaces to his memory module controller, through his associative memory. However, since this language is not in the claims, it is meaningless to discuss it further here. Suffice it to say that if the limitation is added to the claims, the Examiner might consider the associative memory to be part of Levy's system memory controller, since it apparently performs some system memory functions as mentioned above.

Conclusion

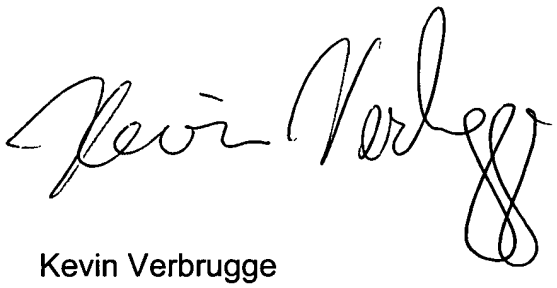
All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning a communication from the Examiner should be directed to the Examiner by phone at (703) 308-6663.

Any response to this action should be labeled appropriately (serial number, Art Unit 2188, and After-Final, Official, or Draft) and mailed to Commissioner for Patents, Washington, D.C. 20231, faxed to (703) 872-9306, or delivered to Crystal Park 2, 2121 Crystal Drive, Arlington, VA, 4th Floor Receptionist.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197.



Kevin Verbrugge
Primary Examiner
3/23/04